Implementation in single ASIC chip, of a Multicarrier SCPC-TDMA Demodulator for a regenerative DVB payload

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Abstract
This paper presents the functionality and performance of an ASIC implementing a digital multi-carrier demultiplexer and demodulator (MCDD) for a Digital Video Broadcasting (DVB) payload.
The multi-carrier demodulator has to be suitable for either single or multiple QPSK continuous (SCPC) and TDMA mode carriers. The system requirements are such that any mixture of 'high' rate (~ 6Mbits/sec) 'low' rate carriers (~2Mbits/sec) is permissible and the carriers access independently and asynchronously. These requirements imply flexible and efficient demodulator architecture implemented by means of VHDL.
The demodulator ASIC receives a 'high' rate carrier at an Intermediate Frequency (IF) equal to ¼ of sampling rate. After the anti-aliasing filter, a single ADC samples the input data at a fixed sampling rate of 14.66MHz. Each 'high' rate carrier is then processed in continuous or TDMA mode.
In case of 'low' rate carriers an input poly-phase filter is activated to demultiplex simultaneously 'three' low rate carriers. These carriers occupy the same bandwidth of a single high rate carrier. All the carriers are simultaneously processed by the demodulator, which provides in this case three data streams.
The specifications about input carrier frequency and power unbalance are severe and require specific attention, especially in TDMA mode.

Algorithms

Introduction
The MCDD should operate either in SCPC or burst mode at four different symbol rates at each mode. The symbol rates are divided in two classes: 'high' rate carriers (approximately 6Mbits/s) and of 'low' rate carriers (2.292Mbits/s). The combination of an integer number of 'high' and/or 'low' rate carriers at the output of the MCDD bank provides an equivalent multi-program DVB compliant transport stream.
'High' rate carriers occupy all the input bandwidth of an MCDD unit operating as a single MCDD. 'Low' rate carriers occupy one third of the input bandwidth so that a single MCDD unit operates as a true MCDD demultiplexing and demodulating three channels simultaneously.
The most stringent specifications are in terms of carrier power unbalance, and carrier frequency offset. The required carrier unbalance was 20 dB, for an implementation loss of 1 dB and an Eb/No of 10.6 dB .This required an accurate arithmetic and filters having long pulse response, then many taps.
The specified input frequency offset was of the order of 12%R_s for the low rate carriers and of 4% R_s for the high rate carriers. This frequency offset had a severe impact on the demodulator operation particularly in TDMA mode and for the low rate carriers, where a burst loss of 10^{-8} is required. In order to meet the burst loss specs, a start of burst detector has been implemented. This

performs an initial coarse estimation of burst timing and carrier frequency offset. After the coarse estimation the synchronization loops can acquire and track the carrier phase and the symbol timing within a residual offset. The structure of the MCDD is shown in Figure 1. It includes the following main blocks: demultiplexer, matched and interpolator filter, carrier frequency synchronizer, carrier phase synchronizer, symbol timing synchronizer, carrier frequency estimator, power estimator for external AGC. A suitable host interface is also foreseen to program the chip and to extract the data.

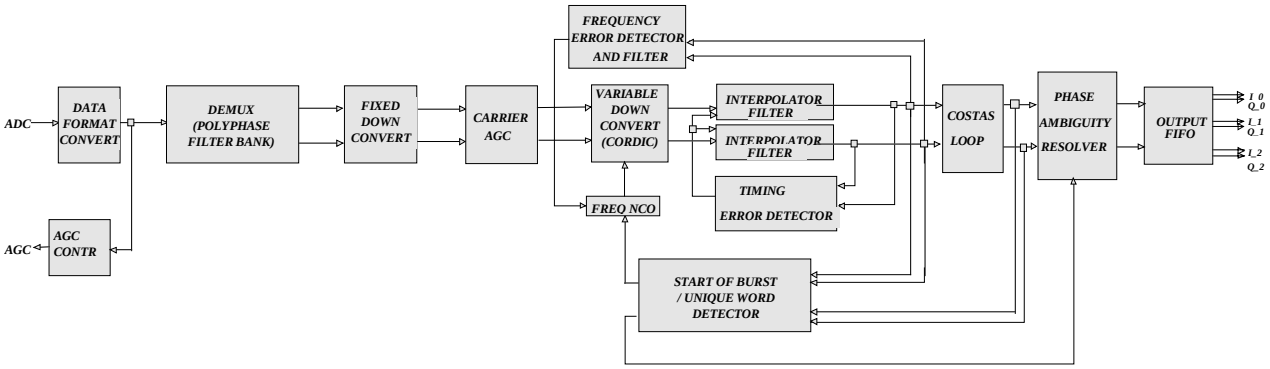

Figure 1 - Hot Bird 5 Demodulator Block Diagram

Symbol synchronizer

The symbol synchronizer is based upon the timing error detector proposed by Gardner. It requires two samples per symbol and operates equally well in SCPC and/or TDMA mode. The detector algorithm is the following:

$$\varepsilon_k = I_{k-1/2} * \left(I_k - I_{k-1}\right) + Q_{k-1/2} * \left(Q_k - Q_{k-1}\right)$$

where k is the symbol number. The values of the pair of symbols lying between the $(k\text{-}1)^{th}$ and k^{th} strobes are $I_{k-1/2}$, $Q_{k-1/2}$. An error sample e_k is generated for each symbol.

The slope of the error detector S-curve depends upon the statistics of the received data. For random data, the detector gain depends upon the pulse shaping roll-off factor and performs best for roll-off factors in the range of $a \in \{0.2\text{-}1\}$.

It is proven that the ε_k is independent of the carrier phase offset, since all terms containing carrier phase information are either canceled or combined to $\sin^2(\Delta\theta) + \cos^2(\Delta\theta) = 1$.

On the contrary ε_k is sensitive to frequency offset. In this case the error detector characteristic given by eq. (1) is multiplied by a $cos(\pi\Delta f)$ factor. Thus, in the presence of frequency offset Δf, the detector error indication is reverted for $\Delta f=1$ Therefore it behaves well until the frequency offset is below $50\%R_s$.

In TDMA mode, considering the frequency estimation scheme employed, the worst case condition occurs just after the start of burst detection, when a residual carrier frequency offset is present. This residual frequency offset is well below the detector's performance upper limits.

Digital interpolator and Squared Root Raised Cosine (SRRC) filter are implemented by and optimized as a single filter. Sixteen phase responses are used for interpolation.

The demodulator clock is fixed at 14.666 MHz, thus the number of samples per symbol at the symbol synchronizer input is variable and depends upon the signal rate. It is an irrational number; i.e. 2.95 samples /symbol for 1.243 Msymbols/s carrier up to 4.43 samples/symbol for the 3.31 Msymbols/s carrier, in TDMA mode. The resulting timing resolution is between 0.0141 to 0.0212 respectively. This imposes a performance degradation between 0.05dB and 0.15dB.

The error detector signal e_k is applied to a first order loop with time variable bandwidth. Three constant loop values are used in order to enhance the loop's acquisition performance and to maintain the steady state timing error variance low.

An approximate analysis of the synchronizer performance gives a worst case implementation loss of 0.25 dB.

Carrier Phase synchronizer

The implemented carrier phase recovery loop is a 2nd order modified Costas loop. The detector algorithm is described by the equation:

$$\varepsilon_k = Q_k * sign(I_k) - I_k * sign(Q_k)$$

It is implemented as a numerical loop and operates at 1 sample/symbol. The final phase estimate is obtained by the 2nd order loop which is controlled by time variant loop constants. Pairs of three constant values are used in order to enhance the loop's acquisition performance and to maintain the steady state phase error variance low. As for the timing loop, these values are set empirically. The initial values assure a fast convergence without making the loop unstable. Thus, the loop's bandwidth is higher in acquisition state and decreases until it reaches its final low value at tracking mode. This assures a low phase error variance.

The following figure summarises the implementation losses of the carrier synchronizer.

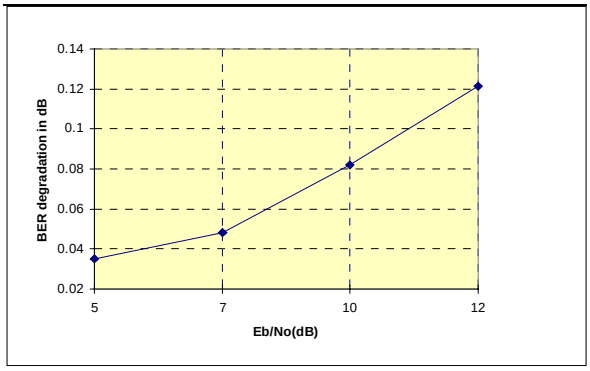

Figure 2: losses of the carrier synchronizer.

Carrier frequency synchronizer

The implemented carrier frequency recovery loop is a 1nd order quadricorrelator. The detector algorithm is described by the equation:

$$\varepsilon_K = Q_k * I_{k-1} - I_k * Q_{k-1}$$

It is implemented as a numerical loop and operates at 1 sample/symbol.

Start of Burst Detector

A Maximum Likelihood derived start of burst detector is implemented. The algorithm was proposed for the synchronization of TDMA - FSK signaling schemes and it is similar to those used for Code Acquisition applied to DS-SSMA systems. It is formulated as follows:

1. An estimation window of L=32 received symbols (I, Q) is taken. These symbols are correlated against the preamble sequence by means of a L/2-point DFT, see Figure 3.
2. A Hybrid MAXimum/ Double Threshold Crossing criterion (MAX/DTC) is used to estimate Δf using sliding windows with step $T_s/2$ where T_s the symbol period.

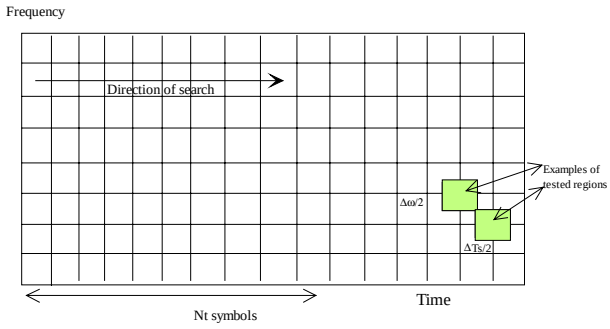

Figure 3: Time - Frequency search region

A MATLAB program was developed to estimate the algorithm's performance.
The results obtained using the MATLAB model have been verified by system simulation for E_b/N_o in the range of 3.5-5.5 dB. Simulations for higher E_b/N_o values are prohibitive in time. Simulation results and estimations are substantially in accordance and are shown in figure 4.

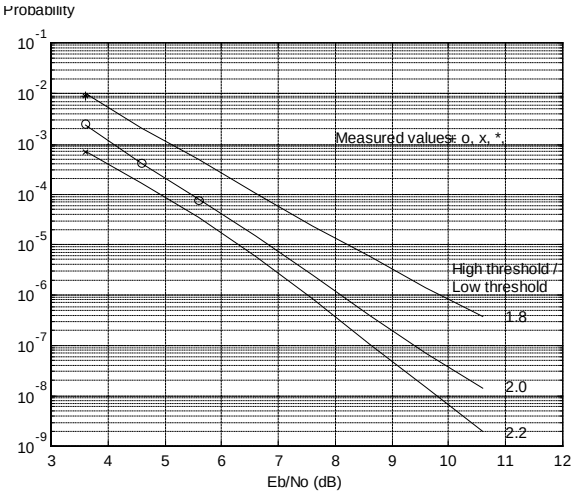

Figure 4 - Burst loss for low rate carriers

Hardware

SKYPLEX HB5 on-board demodulator has been completely implemented using digital technology. The target technology is a MHS, MG1 CMOS family, sea of gates with 0.6 micron channel length, 3 metal layers and 264,375 gates equivalent area.

The ASIC specification to process, either 3 low rate channels, or 1 high rate channel requires the insertion or the bypass of a demultiplexer organized as a polyphase filter. The hardware structure must be able to switch between burst mode for TDMA and continuous mode for SCPC.
In case of low rate carriers the same computation resources are shared in time division.
In general the parameters passed to the ASIC functional blocks are organized as an array of 3 elements which uses one element for each channel. If the ASIC is in high rate channel modality, just the central element of the previous array is used.
Two main phases are foreseen: Initialization and Running. During Initialization the configuration registers are programmed via an external host microcomputer; at the end of this step, the host sends to the ASIC a start command to enter the Running Phase.
During the Running Phase the ASIC is enabled to process the input signal, however many configuration registers can be refreshed to improve the radiation tolerance.

ASIC Top View

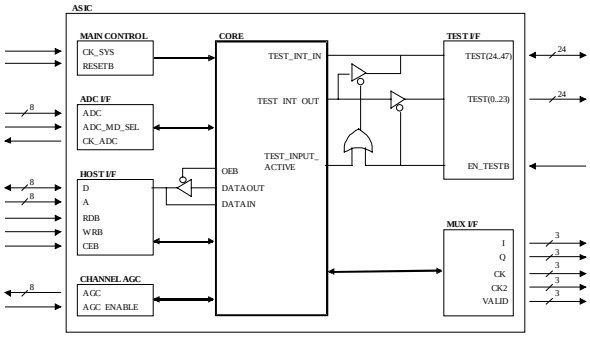

Figure 5: ASIC Block Diagram

The ASIC top view appears as a ASIC CORE surrounded by the i/o interfaces which can be logically divided into the following categories.

MAIN CONTROL includes the Reset and the Master clock.
ADC I/F includes 8 bits ADC data bus coming from the external ADC and the sampling clock.
HOST I/F is a microprocessor like interface containing the classical signals: an 8 bits address bus (A), an 8 bits bi-directional data bus (D), the read and write controls (RDB, WRB) and the chip enable (CEB);
CHANNEL AGC consists of an 8 bits output to be fed to an external DAC and an enable input (AGC_ENABLE).
TEST I/F: consists of a bi-directional bus which can be configured as 48 bits output or 24 bits input; the "output configuration" allows to carry out some internal buses for test purposes only.
MUX I/F: is the chip output, it contains the demodulated bits (I,Q) as well as the clocks (CK, CK2) and the controls (VALID). These signals are differentiated by the 3 channels.

ASIC CORE

The ASIC CORE block diagram is shown hereafter

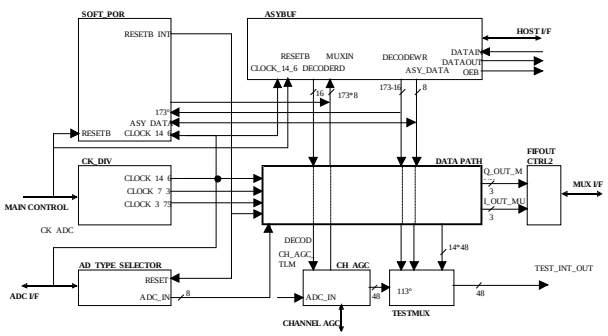

Figure 6: ASIC Core Block

CK_DIV and SOFT_POR blocks are used to create and distribute the clocks and the reset. Inside the ASIC four clocks are present to adapt the processing rate of the different blocks to the requirements.
AD_TYPE_SELECTOR block is intended for ADC data type selection.
ASYBUF block is for the host interface.
CH_AGC block implements a channel AGC based on three working modes: open loop: quasi-open loop, closed loop mode.
TESTMUX implements a multiplexer with 14, 48 bits input, and a single 48 bits output which can be selected writing a control register via the host interface.
FIFOUT and CTRL2 implement the output stage of the demodulator: the demodulated bits are sent to the output in serial fashion and grouped as 16 bits blocks with the related controls (CK, CK2 and VALID, one for each channel).
DATA PATH is the modem signal processing: it basically implements the functions summarized in figure 1.

Conclusion

An ASIC was implemented to implement a digital multi-carrier demodulator suitable for continuous-burst mode signals used in a regenerative payload for Digital Video Broadcasting (DVB) applications. The ASIC processes QPSK modulated continuous carriers (SCPC) and burst carriers (TDMA) at 4 different data rates in several combinations and with low implementation loss. The ASIC basically includes demultiplexer, matched and interpolator filter, carrier frequency synchronizer, carrier phase synchronizer, symbol timing synchronizer, power estimator, start of burst estimator host interface.
The ASIC is implemented in Radiation Tolerant 0.5 μm SI-CMOS process and its complexity is about 190Kgates.

Thanks

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