MULLTI-CARRIER DEMODULATOR ASIC DESIGN FOR THE SKYPLEX 2ND GENERATION ONBOARD PROCESSOR

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1 Abstract

This paper presents the functionality and performance of the Multi-Carrier Digital Demodulator (MCDD) ASIC developed for the Skyplex 2nd generation on board processor to be embarked on the Hot Bird V satellite. The Skyplex 2nd generation processor will provide commercial DVB compliant services, i.e. DTH DTV, Internet 'Push' and multimedia applications, within the Hot Bird V coverage area, [1-6].
The demodulator ASIC has to cope with QPSK continuous (SCPC) and TDMA burst mode carriers. The system requirements are such that any mixture of 'low' (2Mbit/s) and 'high' (6Mbit/s) carriers is permissible and the carriers access independently and asynchronously, [4]. These requirements imply flexible and efficient demodulator architecture.
The developed demodulator ASIC receives a 'high' rate carrier at an Intermediate Frequency (IF) equal to the symbol rate. After the anti-aliasing filter, a single ADC samples the input data at –at least four samples per symbol –the sampling clock is fixed at 14.6 MHz independently from the carrier and the timing recovery is asynchronous with respect to the input carrier symbol rate. Each 'high' rate carrier either in continuous or burst mode is then demodulated.
In case of 'low' rate carriers, an input poly-phase filter is activated to demultiplex 'three' carriers. Three 'low' rate carriers occupying the bandwidth of a single 'high' rate carrier are simultaneously processed by the demodulator, which provides the respective transport streams. Moreover, all three 'low' rate carriers may be either simultaneously active or not.

The paper discusses the MCDD functional performance at system level focusing on the most critical issues of the multi-rate operation and the implementation of the synchronisation algorithms. It provides the ASIC hardware description and discusses the aspects of dual VHDL, C++ modelling and co-simulation aspects.

2 MCDD Functional description and performance assessment

2.1 Introduction

The MCDD should operate either in SCPC or burst mode at four different carrier rates at each mode, [4]. The symbol rates are divided in two classes:

- 'high' rate carriers (approximately 6Mbits/sec) and
- 'low' rate carriers (2.292Mbits/sec).

The combination of an integer number of 'high' and/or 'low' rate carriers at the output of the MCDD bank provides an equivalent multi-program DVB compliant transport stream. The combination of operating rates used for the Skyplex 2nd generation processor, for the SCPC mode, are depicted in Table 1, [4].

FEC	'High' rate carriers	'Low' rate carriers
r = 3/4	6 x 6.875	0
	5 x 6.875	3 x 2.291
r = 2/3	6 x 5.632	0
	5 x 6.758	0
	4 x 6.875	4 x 2.291
r = 1/2	4 x 6.875	0
	3 x 6.875	3 x 2.291
	2 x 6.875	6 x 2.291

Table 1 [4] Access bit rates per SCPC channel. In burst mode, the rates are multiplied by the factor 52/48.

'High' rate carriers occupy all the input bandwidth of an MCDD unit operating as a single MCDD. 'Low' rate carriers occupy one third of the input bandwidth so that a single MCDD unit operates as a true MCDD demultiplexing and demodulating three channels simultaneously.

It is to be mentioned that the developed MCDD can operate with all possible combinations of 'high' and 'low' rate carriers –not included in Table 1, satisfying the above mentioned bandwidth occupancy constraint.

The most stringent specifications are in terms of carrier power unbalance, and carrier frequency offset. The carrier unbalance is 20 dB for an implementation loss of 1 dB and an E_b/N_o of 10.6 dB. This required an accurate arithmetic and filters having long pulse response, then many taps.

The specified input frequency offset is of the order of 12%R_s for the low rate carriers and of 4% R_s for the high rate carriers where R_s is the symbol rate. This severely impacts on the demodulator operation particularly in TDMA mode and for the 'low' rate carriers, where a burst loss of 10^{-8} is required. In order to meet the burst loss specs, a Start of Burst Detector (SOBD) is used. The SOBD also performs an initial coarse estimation of burst timing and carrier frequency offset. Thus, frequency offset estimation is implemented separately in such a way that the carrier

phase and timing estimators can acquire and track within the range of the residual frequency offset.

The structure of the MCDD is shown in **Error! Reference source not found.**. It consists of:

- the demultiplexer and matched –interpolator filters,
- the carrier frequency offset, the carrier phase and symbol synchronisers,
- the UW and Start of Burst detectors,
- the power estimator for external AGC and
- the host interface.

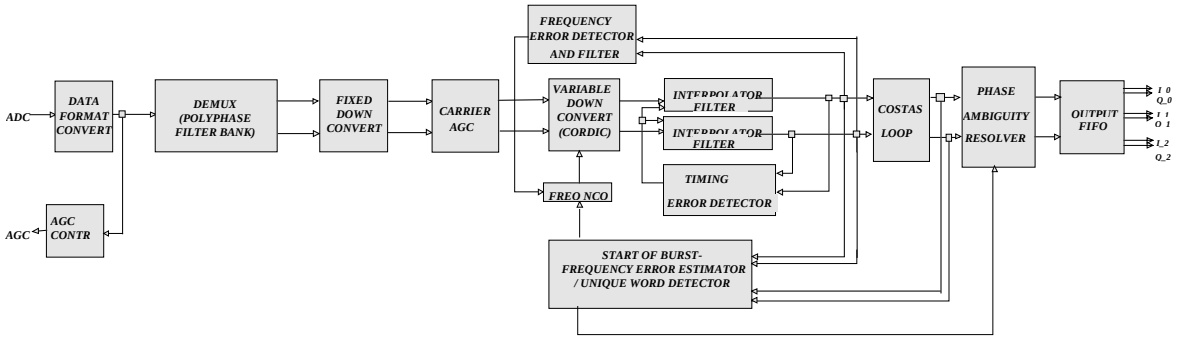

Figure 1 MCDD Functional Block Diagram

It requires two samples per symbol and operates equally well in SCPC and/or TDMA mode. The detector detector is described by the following equation:

$$\varepsilon_k = I_{k-1/2} * \left(I_k - I_{k-1}\right) + Q_{k-1/2} * \left(Q_k - Q_{k-1}\right) \quad (1)$$

where k is the symbol number. The values of the pair of symbols lying between the $(k\text{-}1)^{th}$ and k^{th} strobes are $I_{k-1/2}$, $Q_{k-1/2}$. An error sample ε_k is generated for each symbol.

2.2 Symbol synchroniser

The symbol synchroniser is based upon the Gardner timing recovery algorithm [7]. Figure 2 shows its simplified block diagram.

An error sample ε_k is generated for each symbol. The slope of the error detector S-curve depends upon the statistics of the received data. For random data, the detector gain depends upon the pulse shaping roll-off factor. For random data, the detector gain depends upon the pulse shaping roll-off factor. As a matter of fact the detector performs best for roll-off factors in the range of $a \in \{0.2\text{-}1\}$. The Skyplex processor roll-off factor is 0.33, [1, 4].

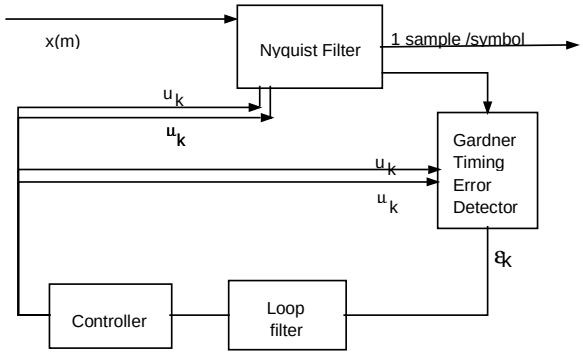

Figure 2 Simplified block diagram of the symbol synchroniser.

It is proven in [7] that the ε_k is independent of the carrier phase offset, since all terms containing carrier phase information ($\Delta\theta$) are either cancelled or combined to $\sin^2(\Delta\theta) + \cos^2(\Delta\theta) = 1$. Therefore, the timing loop can lock prior to locking of the carrier phase loop. Besides it is rather robust to frequency offset and it could operate without any previous frequency adjustment. In presence of frequency offset Δf, the error detector indication is reverted for $\Delta f = 50\%R_s$ and the timing loop behaves well below this value.

The digital interpolator and the Squared Root Raised Cosine (SRRC) filter are implemented by and optimised as a single filter. The ideal SRRC shaping is taken as a reference. Sixteen phase responses are used. The input and output signal are quantized to 8 bit each.

The demodulator clock is fixed at 14.666 MHz, thus the number of samples per symbol at the symbol synchroniser input is variable and depends upon the signal rate. It is an irrational number; i.e. 2.95 samples/symbol for 1.243 Msymbols/sec carrier up to 4.43 samples/symbol for the 3.31 Msymbols/sec carrier, in TDMA mode. The resulting timing resolution is between 0.0141 to 0.0212 respectively. This imposes performance degradation between 0.05dB and 0.15dB.

The error detector signal ε_k is applied to a first order loop with time variable bandwidth. Three constant loop values are used in order to enhance the loop's acquisition performance and to maintain the steady state timing error variance low. These values are set empirically. The initial values assure a fast convergence without making the loop unstable. The final value of the loop constant is a trade off between the bias and timing variance of the estimation. Figure 3 depicts the evolution of the timing loop constant. Figure 4 illustrates the timing recovery loop output in TDMA mode.

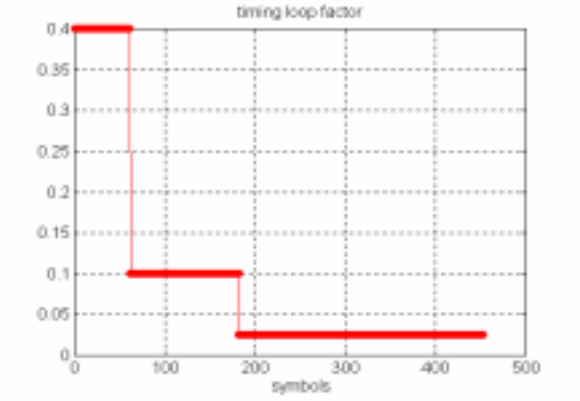

Figure 3 Evolution of the loop factor k1

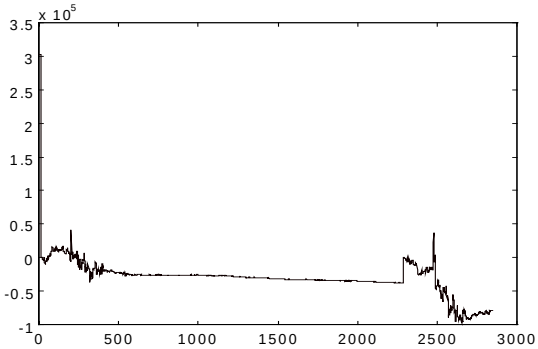

Figure 4 TDMA Mode Time Response (Accumulator value)

The performance degradation due to the symbol synchroniser at tracking mode is caused by the mean timing error and its variance while operating within the residual frequency offset range –see § below. The timing error variance is proportional to the loop bandwidth and it is of the order of 1.6×10^{-4}. Finally, the overall performance degradation at the operating point of E_b/N_o =10.6 dB, considering also the variable timing resolution, is less than 0.25dB –for the 'low' rate carriers.

2.3 Carrier Phase synchroniser

The implemented carrier phase recovery loop is a 2nd order modified Costas loop, [13]. The detector algorithm is described by the equation:

$$\varepsilon_k = Q_k * sign(I_k) - I_k * sign(Q_k) \qquad (2)$$

It is implemented as a numerical loop and operates at 1 sample per symbol. The final phase estimate is obtained by the 2nd order loop which is controlled by time variant loop constants. Pairs of three constant values are used in order to enhance the loop's acquisition performance and to maintain the steady state phase error variance low. As for the timing loop, these values are set empirically. The initial values assure a fast convergence without making the loop unstable. Thus, the loop's bandwidth is higher in acquisition state and it decreases until it reaches its final low value at tracking mode. This assures a low phase error

variance. Figure 5 depicts the evolution of the phase loop constants. Figure 6 illustrates the carrier phase recovery transients in TDMA mode.

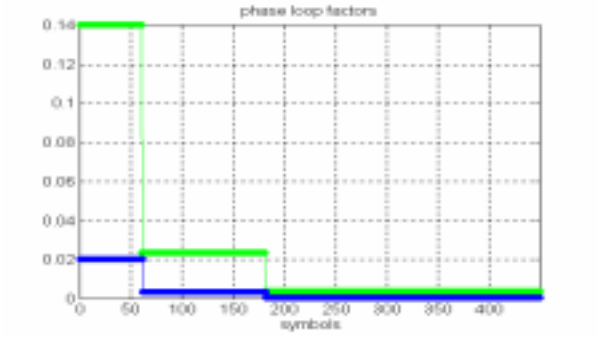

Figure 5 Evolution of the phase loop constants

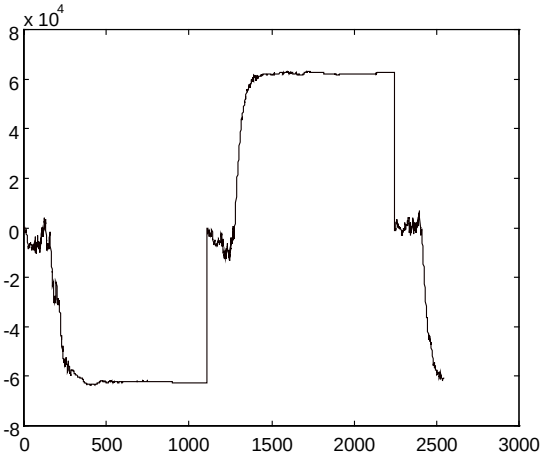

Figure 6 TDMA mode: Frequency Error Accumulator in Costas Loop with residual frequency error ±18 KHz, versus the number of symbols.

The performance degradation due to the phase error variance is assessed for the studied 2nd order Costas loop in tracking mode.[1] Figure 7 shows the BER degradation and vs E_b/N_o(dB).

[1] In acquisition state, the phase error variance and consequently the phase deviation are higher. However, the phase deviation remains lower than 6.5°, resulting in a performance degradation less than 0.5dB. Note that the synchroniser is not a Decision Derived one and thus any symbol error during the acquisition mode does not affect directly the synchronisation procedure.

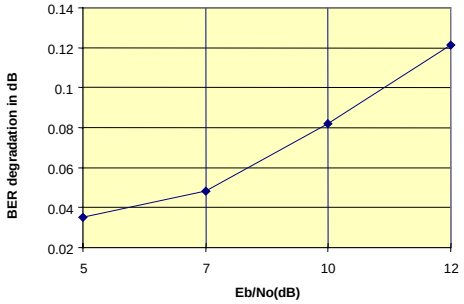

Figure 7 BER performance degradation $L_{s\theta}{}^2$ in the presence of phase error variance of the studied loop in tracking mode.

Furthermore, quantisation causes a maximum phase estimation bias of $bias_\theta = \Delta\theta/2 = \pi/2^b$. For 8 quantization bits, $bias_\theta \approx 0.71°$resulting in performance degradation L_{bias} of the order of 0.11dB. Finally, $L_{tot,\theta} = L_{s_\theta}{}^2 + L_{bias,\theta} \leq 0.21dB$ at the operating point of E_b/N_o =10.6 dB –for the 'low' rate carriers.

2.4 Start of Burst Detector - Carrier Frequency estimator

2.4.1 TDMA mode

A Maximum Likelihood derived estimator is implemented to determine start of burst. It also performs coarse frequency offset estimation during the preamble. The algorithm is proposed for the synchronization of TDMA - FSK signaling schemes and it is similar to those used for Code Acquisition applied to DS-SSMA systems [17-19]. It is formulated as follows:

- An estimation window of L=32 received symbols (I, Q) is taken. These symbols are correlated against the known preamble sequence by means of a L/2-point DFT,
- A Hybrid MAXimum / Double Threshold Crossing criterion (MAX/DTC) is used to estimate accurately $\Delta f' \in \{-144KHz \ \ to \ \ 144KHz\}$ using sliding window with step $T_s/2$ where T_s the symbol period.

All test variables; i.e. DFT bins are compared and the maximum is selected according to the MAX criterion; defined as follows:

MAX criterion: choose test variable $bin^{(j)}$ if $bin^{(j)} > bin^{(i)}$ for j=1,2,…,L/2 and I ≠j (3.4.1)

Then, the selected bin is compared to a first threshold x_1. If the threshold x_1 is crossed, the hypothesis of having acquired is made. In order to enhance the miss detection and the false alarm avoidance, a double TC criterion is used with a second threshold x_2. The double TC criterion can be defined as:

TC criterion 1: if $bin^{(j)} > x_1$ then $\Delta f' = (bin)^{(j)}$ else perform TC criterion 2 (3.4.2)

TC criterion 2: if $bin^{(j)} > x_2$ then

if $((bin^{(l)} + bin^{(l+1)}) > x_1$ or $(bin^{(l)} + bin^{(l-1)}) > x_1)$ then

$$\Delta f' = (bin^{(l)} + bin^{(l+1)}) \text{ or } \Delta f' = (bin^{(l)} + bin^{(l-1)})$$

where x_1, x_2 the two thresholds such that $x_1 > x_2$.

A MATLAB program is developed to simulate the algorithm's performance. The MAX search is performed for the uncertainty region in the two-dimensional frequency × time domain defined by the number of used DFT bins and a sufficient number of tested symbols; i.e. k*L/2. Considering the uncertainty region shown in Figure 8, each small rectangle of $\Delta f \times \Delta T_s$ is defined as a cell. The estimation procedure described above is equivalent to finding out which cell satisfies the MAX/DTC criterion.

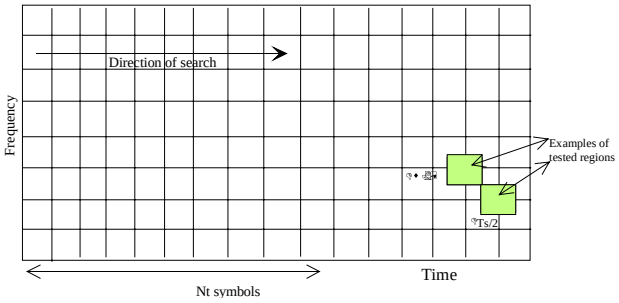

Figure 8 Time ´ Frequency uncertainty region

The maximum estimation error corresponds to the DFT resolution and is $|\Delta f|_{res} \leq 18KHz$. This corresponds to a worst case normalised residual frequency offset of $|\Delta f|_{res} \leq 1.5R_S\%$ *and* $|\Delta f|_{res} \leq 0.55R_S\%$ for the low rate and high rate carriers respectively, which is well into the range of operation of the phase recovery loop.

The estimator performance is given by the probability of carrier frequency acquisition failure shown in Figure 9 versus E_b/N_o*(dB)* for various pairs of threshold values. The specified parameter of the Probability of Burst Loss (1×10^{-8}) is the one compared with the above mentioned carrier frequency acquisition failure probability.
The results plotted correspond to the worst case conditions; i.e. 'low' rate carriers with maximum $\Delta f' = \pm 138KHz$ and they are in agreement with those obtained by measurement using the overall system simulator where filtering and finite arithmetic effects are included.[2] Impairments due to the timing error and quantization are also considered.

The probability of acquisition failure is a function of the threshold pairs. The results given above indicate the range of the threshold pairs values minimising the failure probability.

[2] The results obtained using the MATLAB model are verified by system simulation for $E_b/N_o < 10.6dB$ values; i.e. in the range of 5-6dB. Even for low E_b/N_o values the simulation running time is very long in order to obtain meaningful results. Results for higher E_b/N_o values require prohibiting running time.

For appropriately selected threshold pairs, the failure probability remains lower than 10^{-8} for $E_b/N_o>10.6dB$.

Furthermore, in real operative conditions the burst-to-burst frequency offset may result well below the worst case value used in the algorithm performance evaluation. Consequently, the presented results are to be considered as the upper performance limits in terms of probability of acquisition failure.

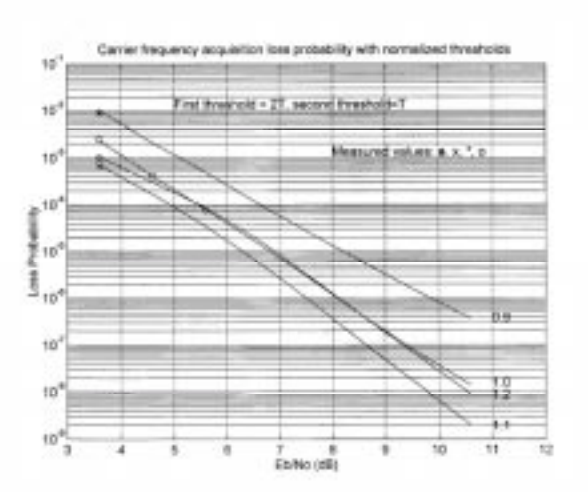

Figure 9 Probability of carrier frequency acquisition failure; low rate carriers; maximum input frequency offset ΔF=±138KHz.

3 ASIC Hardware description

The MCDD ASIC has been implemented using digital MHS technology. The device is based on a see of gates approach and its main characteristics are: CMOS technology, 0.6 micron channel length, 264,375 equivalents gates, 3 metal layer. The ASIC is fully programmable from a system level parameters point of view: 172 registers can be write to set the appropriate operating mode and 16 telemetry values can be read. The operating modes can be divided into two main classes: single high rate channel or triple low rate ones. The modality exchange is obtained inserting or bypassing a demultiplexer based on a polyphase filter. Furthermore the hardware structure is able to manage both SCPC or TDMA input signals, at different time in the high rate modality and at the same time, on different channels, in the low rate one. The ASIC initialization can be done via an host microcomputer which also gives the start elaboration. During the running phase many registers can be refreshed to improve the radiation tolerance.

The ASIC top view appears as a CORE which contains the data path and a some i/o interface. The i/o interfaces consist of an 8 bits ADC input, an host interface (an 8 bits data bus, an address bus and the controls), an AGC output and an output interface which delivers the demodulated bits and the related clocks. A further useful i/o interface is a 48 bits parallel test bus which allows to read internal partial results or to inject input data to the internal stages.

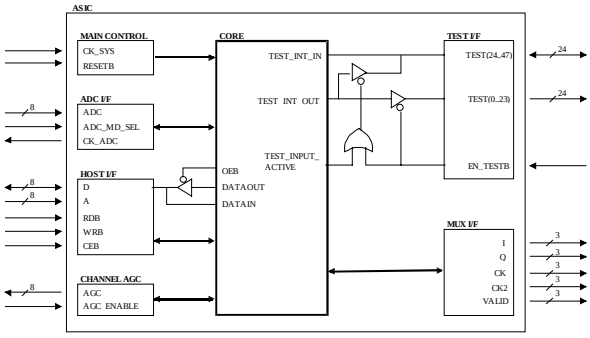

Figure 10 - ASIC Top View

The ASIC CORE implements the signal processing (data path in the figure) including also some auxiliary functions as power-on-reset, clock division and distribution, ADC data adaptation and finally i/o manage in terms of address decoding, test signals multiplexing and so on.

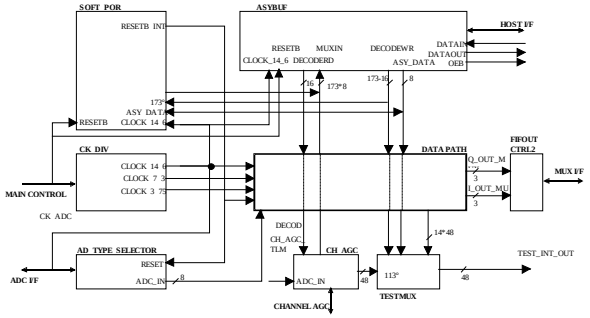

Figure 11 - ASIC CORE

The data path processes the signal implementing all the functions summarised in the ASIC block diagram given in fig.1. The main functional blocks are a polyphase filter, a matched and interpolator filter, the frequency, phase, timing and symbol synchronisers, and a start of burst detector. The arithmetic circuits are shared for the three channel in the low rate modality whereas the memory ones are keep separated to store the states of the calculus (filters, loop, and so on). A double rate approach is used to obtain a further hardware reduction, so a single arithmetic circuit, in many cases, performs two computations inside the same sample period.

4 Conclusion

An ASIC has been realised to obtain a MCCD which is able to process both a continuos and burst mode signal in both SCPC and TDMA modalities. The application field is closely related to the DVB area for regenerative payloads. The rad-hard technology chosen for the device is the 0.6 micron CMOS MHS in the 264,375 gates size.

Thanks

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